U.S. Express Mail No. EL492178688US
Filing date: 03-03-01

Patent
TKHR Docket No. 50321-1920
99RSS406

PHASE ADJUSTABLE POLYPHASE FILTERS

INVENTORS

ALYOSHA MOLNAR

RAHUL MAGOON

BACKGROUND OF THE INVENTION

1. Field of the Invention.

This invention relates to polyphase filters for wireless communication systems, and more particularly, to polyphase filters having adjustable phase for obtaining accurate quadrature in digital cellular telephone systems.

2. Related Art.

Modern wireless communication systems such as digital cellular telephone systems send and receive signals by encoding and decoding information on a radio frequency carrier with phase components that can be mapped on an I-Q plane. Such systems need high-accuracy phase splitters to produce accurate quadrature for modulation in radio transmitters. High accuracy phase splitters are also needed for demodulation in radio receivers. Such phase splitting is often accomplished through the use of polyphase filters.

Many polyphase filters only produce an accurate phase split over a narrow frequency range, and even polyphase filters with wide-band phase splitting characteristics are only as accurate as the matching of the electrical parameters of their passive components. Good matching requires devices that are large in size in the context of cellular telephones, for example, and suffer from increased parasitic losses that degrade noise performance and consume more power,

shortening already limited battery life. Furthermore, other circuits in the radio receiver besides the phase splitter itself can alter the phase and introduce errors in quadrature. Such errors are typically small (on the order of 5 degrees), but industry requirements are on the order of 2 to 3 degrees or less, so even small errors can present a problem.

SUMMARY

This invention provides polyphase filters that maintain accurate quadrature in communication equipment. The filters have at least two-phase splitters and a variable resistance on an output of at least one phase splitter, and preferably all phase splitter outputs. The variable resistor can take any suitable form, such as a MOS transistor biased in the linear (triode) region, a bipolar differential transistor pair, a digitally switchable resistance, or the like. The phase adjustment required for a particular filter or system can be identified through a calibration process in either a closed loop system or an open loop system, and the phase of each phase splitter can be adjusted accordingly.

The polyphase filter can also include four phase splitters that produce differential outputs. In that case, a variable resistance is provided for one or both differential outputs. While a 90E phase shift is typical, the invention is applicable to systems which use a 45E phase shift or any other phase shift, and of course phase errors in the entire communication device can be corrected using this invention.

Other systems, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional

systems, methods, features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWING

The invention can be better understood with reference to the following figures. The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principals of the invention. Moreover, in the figures, like reference numerals designate corresponding parts throughout the different views.

FIG. 1 is a block diagram of a communication system using quadrature phase modulation having phase components on an I-Q plane.

FIG. 2 is a diagram of the I-Q plane used in a quadrature phase modulation system.

FIG. 3 is a circuit diagram of a polyphase filter having variable resistors for phase adjustment.

FIG. 4 is a circuit diagram of a differential polyphase filter having variable resistors for phase adjustment.

FIG. 5 is a block diagram of phase error detection and correction circuitry in a communication device.

FIG. 6 is a diagram of a closed loop phase error detection and correction system in a communication device, using a MOSFET as a variable resistor.

FIG. 7 is a diagram of a communication device having an open loop phase error detection and correction system, using a MOSFET as a variable resistor.

FIG. 8 is a circuit diagram of a variable resistance circuit that uses a bipolar differential pair of transistors.

FIG. 9 is a circuit diagram of a variable resistance circuit that is digitally switchable.

FIG. 10 is a block diagram of a digitally controlled variable resistance circuit.

DETAILED DESCRIPTION

In Fig. 1, a communication system includes at least one base station 100, and at least two user stations 102, 104. The base station and each user station each have a radio frequency transmitter and receiver, and the user stations 102 communicate with the base station 100 over designated radio frequency channels, using phase modulation, by orthogonally encoding the carrier frequency with signal points having phase components on an I-Q plane, shown in Fig. 2.

The I-Q plane has several signal points, including 1,0 and 0,1 in Fig. 2. In order to be properly decoded, the correct phase difference between the I component and the Q component must be maintained. This phase difference could be 90E or any other suitable phase difference. In the receiver, this phase difference is established using a polyphase filter.

In Fig. 3, a polyphase filter 300 having an input terminal 302 includes a resistor 304 and a series capacitor 306 tied to the input terminal 302 on one end and to ground 308 on the other end. A capacitor 310 and series resistor 312 are also tied to the input terminal 302 on one end and ground 308 on the other end. These are single-ended outputs.

Each RC network (304, 306 and 310, 312) splits the phase of an incoming signal, such as a local oscillator tone, so that the phase of the signal at an output port 314 is approximately 90E out of phase with a signal produced at an output port 316. In fact, if all of the respective resistances and capacitances are identical,

then the outputs will be exactly 90E out of phase, which is ideal. The unloaded outputs 0_{314} and 0_{316} at the ports 314, 316, respectively can be expressed as follows:

$$O_{314(UNLOADED)} = input \frac{1}{1 + j\omega R_{304} C_{306}}$$

$$O_{316(UNLOADED)} = input \frac{j\omega R_{312} C_{310}}{1 + j\omega R_{312} C_{310}}$$

As seen above, if $R_{304} = R_{312}$ and $C_{306} = C_{310}$, then O_{314} and O_{316} are exactly 90E out of phase with each other. However, if the resistive and capacitive values of the filter are not identical, or if external loads 318, 320 do not have identical impedance characteristics, the outputs will not have ideal phase shifts. In a digital cellular telephone system, for example, unequal phase shifts cause inaccurate quadrature, resulting in poor reception.

In order to compensate for inaccurate quadrature due to unequal phase shifting, a variable resistor 322 is provided between the output 314 and ground, and a variable resistor 324 is provided between the output 316 and ground. The resistors 322, 324 can be adjusted to correct for unequal phase shifting.

The loaded outputs O_{314} and O_{316} can be expressed as follows:

$$O_{314(LOADED)} = input \frac{(R_{322} \_ R_{318})}{(R_{322} \_ R_{318}) + R_{304} + j\omega C_{306} R_{304} (R_{322} \_ R_{318})}$$

$$O_{316(LOADED)} = input \frac{j\omega C_{310} R_{312} (R_{324} \_ R_{320})}{(R_{324} \_ R_{320}) + R_{312} + j\omega C_{310} R_{312} (R_{324} \_ R_{320})}$$

By adjusting the resistors R_{322} and R_{324} appropriately, a 90E phase shift can be maintained between O_{314} and O_{316}. This adjustment can be made on the fly, as will be seen.

It can be seen in Fig. 3 that the variable resistance can be connected in parallel with the resistor in the phase splitter, as with the variable resistor 324

(connected in parallel with the resistor 312), or the capacitance in the phase splitter, as with the variable resistor 322 (connected in parallel with the capacitor 306). Of course, both variable resistors could be connected across either the resistor or capacitor of their respective phase splitters, if desired. Also, only one variable resistor is necessary to practice the invention, although two variable resistors probably provide more even loading and better symmetry.

A differential load phase splitter 400 is shown in Fig. 4. The phase splitter 400 includes a plurality of series RC networks connected to each other in series. The first RC network includes a resistor 402 and a capacitor 404, and the second RC network has a resistor 406 and a capacitor 408. The third RC network includes a resistor 410 and a capacitor 412, and the fourth RC network has a resistor 414 and a capacitor 416.

A differential input 418, 420 is provided. The input 418 is applied between the resistor 406 and the capacitor 408, and the input 420 is applied between the resistor 414 and the capacitor 416 in Fig. 4. Terminals 417 and 419 are at virtual ground potential. The phase splitter 400 produces 0E, 90E, 180E and 270E phase shifts as shown.

The phase splitter 400 provides two differential signals to loads 421, 423 at output terminals 422, 424 and 426, 428, respectively. A variable resistor 430 is connected across the output terminals 422 and 424, and a variable resistor 432 is connected across the output terminals 426 and 428. The phase splitter 400 also produces a 90E phase shift in this configuration, although of course circuits that produce 45E and other phase shifts could also be used with this invention.

The manner in which the invention is used to correct phase errors is shown in Fig. 5. A local oscillator signal 500 is applied to a polyphase filter 502. At least one variable resistor 504 is provided for phase correction. The output of the

resistor is applied to multipliers 506, 508 to produce a Baseband I output 510 and a Baseband Q output 512 when mixed with a coded RF signal. The outputs 510 and 512 are decoded by circuitry that is not shown.

The outputs 510, 512 are also fed back to a phase detector 515 that measures any undesired difference in the relative phases of the outputs 510, 512. The phase difference is measured when a test RF signal 514 is applied to the multipliers 506, 508. The phase difference is stored in an error signal memory 516 until the test RF signal 514 is applied again. The test RF signal can be generated internally by a switched tone generator or the like, or it could be contained in a signal received through an antenna.

The test signal can be applied as often as desired. In time division multiple access (TDMA) systems, for example, actual transmission/reception only occurs about 12% of the time, so phase measurements can easily be made between transmissions/receptions.

A phase splitter 600 is shown in a closed loop system for phase correction in Fig. 6. The phase splitter 600 is similar to the phase splitter 400, as will be seen. In this embodiment, the output of a local oscillator 601 is connected to input terminals 417, 419 and variable resistors 603, 605 are connected across the terminals 428, 426 and 422, 426, respectively.

In this embodiment, the resistors 603, 605 are MOS transistor devices. The drain and source of the transistor 603 are connected across terminals 428, 426, and the drain and source of the transistor 605 are connected across terminals 422, 426.

The output terminals 428, 426 represent the I quadrature, and are processed through a mixer 602 and baseband circuitry 604, to an output 606. Similarly, the output terminals 422, 426 represent the Q quadrature signals, and they are processed through a mixer 608 and baseband circuitry 610 to an output 612.

A phase detector 614 compares the outputs 606 and 612. The output of the phase detector 614 is integrated at 616, and the output of the integrator 616 is processed in a differential amplifier 618. The positive output of the differential amplifier 618 provides the gate signal for the variable resistor 603, and the negative output of the differential amplifier 618 provides the gate signal for the variable resistor 605.

A test RF signal source 620 inputs a carrier to the mixers 602, 608, through an amplifier 622. The RF signal is typically a digital cellular telephone or other communication signal, or an internal tone generator, as previously described. The multiplier 602 produces the I quadrature signal by multiplying the RF input signal with the in phase local oscillator signal, and the mixer 608 produces the Q quadrature signal by multiplying the RF input signal by the quadrature phase local oscillator signal. The transistors 603, 605 preferably operate in their linear range. The effective resistance of the transistors is determined by the differential amplifier 618.

A phase splitter 500 is shown in an open loop system for phase correction in Fig. 7. This embodiment is similar to the closed loop system of Fig. 6, but a storage device such as a capacitor 700 bridges the positive and negative outputs of the differential amplifier 618.

The capacitor 700 stores a charge when switches 702 are closed, and holds the charge when the switches 702 are opened. In this manner, the system operates in a closed loop to calibrate, and an open loop during operation. The switches 702 can be controlled fairly independently, and can be closed at periodic time intervals, when temperatures change sufficiently, etc.

This invention is typically sold as part of an integrated circuit chip or chip set. In the open loop system of Fig. 7, for example, such a chip set might also

include an analog to digital converter 704 which converts the I and Q baseband outputs 606, 612 to digital signals, a digital signal processor (DSP) 706 of known design, and a digital to analog converter 708 that produces an output 710 for analog signals. The digital output of the DSP 706 could be the output, as well. In all, these circuits generally complete the receiver circuitry. The chip set can also include circuitry for transmitting signals, including an input circuit 712, such as a microphone or keyboard, an analog to digital converter 714 that feeds a digital signal to the DSP 706, a digital to analog converter 716 and an RF signal generator 718 that produces and transmits the modulated signal.

Figs. 6 and 7 show circuits in which the variable resistor is a MOS transistor such as a MOSFET, but various other configurations could be used. Fig. 8 shows a variable resistor 800 that includes a bipolar differential pair of transistors 802, 804 having their collectors connected to a power source Vcc and their emitters connected to the capacitor 700 in Fig. 7, the differential amplifier 618 in Fig. 6, or any other suitable bias adjustment device. The base of transistor 802 is connected to a terminal of a phase splitting filter (such as terminal 422 in Fig. 4) through a resistor 806. The base of transistor 804 is connected to another terminal of a phase splitter (such as terminal 424 in Fig. 4) through a resistor 808. The bases 806, 808 are also connected to each other by a resistor 810. Changes in the voltage at the emitters cause changes in the effective resistance across the terminals 422, 424.

Fig. 9 shows a variable resistor 900 that is digitally controlled. The variable resistor 900 includes a resistor 902 which is tapped at several points by transistors 904, 906, 908 and 910, to change the total resistance across terminals 422, 424 or the like. By selectively turning the transistors 904, 906, 908 and 910

on and off by controlling the transistor gates (through circuitry not shown), the resistance across terminals 422, 424 can be adjusted.

An analog-to-digital converter (ADC) 1002, a latch 1004, and a digital-to-analog converter (DAC) 1006 could be used instead of the integrator 616, differential amplifier 418 and capacitor 700 in Fig. 7, if desired, as seen in Fig. 10. The analog to digital converter 1002 is connected to the phase detector 614, and the latch 1004 stores the digital value determined by the ADC 1002. The analog output of the DAC 1006 is fed to the variable resistors 603, 605 in Fig. 7. Generally, digital storage is well suited for power on and reset processes in Time Division Multiple Access (TDMA) systems.

In operation, an RF test signal from the source 514 (Fig. 5) is mixed with the local oscillator signal 500 in mixers 506, 508, to produce a baseband or intermediate frequency (IF) signal having I and Q components 510, 512. The phase of the I and Q components is detected in the phase detector 515, and if the phase difference is not 90E, the error signal is stored in memory 516, which adjusts the variable resistors 504 to adjust their effective resistance. In Figs. 6 and 7, for example, the transistors 603, 605 are biased in their linear or triode range, so that even small changes at their gates produce effective resistance changes across their drains and sources, slightly adjusting the phases of the I and Q signals from the local oscillator 500. After phase adjustment on RF carrier signal encoded with a voice communication, data communication or the like is mixed with the phase adjusted local oscillator signals and decoded.

While the various embodiments of the application have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations are possible that are within the scope of this invention.

Accordingly, the invention is not to be restricted except in light of the attached claims and their equivalents.

5